CLAIMS

1. A chip arrangement comprising a first chip which has at least one first signal interface with first coupling elements arranged along a first line in a first number density and at least one second chip which has at least one second signal interface with second coupling elements arranged along a second line in a second number density,

- in which the first signal interface is provided along an edge of the first chip and the second signal interface is provided along an edge of the second chip,

- in which the first and second coupling elements are adapted to permit contactless signal transmission between the first and second signal interfaces,

- in which the first and second chips are so arranged relative to each other that coupling elements of the first and the second signal interfaces can contactlessly transmit signals with each other, wherein said edges of the first and second chips are arranged in mutually facing relationship,

- in which the longitudinal extent of at least one of the signal interfaces along the line associated therewith is greater than the length of the overlap of the two longitudinal extents, wherein said overlap is the distance which the projection of the first longitudinal extent on to the second longitudinal extent has in common with the second longitudinal extent,

- and in which one of the signal interfaces has a greater number density of coupling elements than the other.

2. A chip arrangement comprising a first chip which has at least one first signal interface with first coupling elements arranged along a first line in a first number density and at least one second chip which has at least one second signal interface with second coupling elements arranged along a second line in a second number density, and a coupling component which on a substrate has a coupling unit with third coupling elements arranged along a third line in a third number density and fourth coupling elements

arranged along a fourth line in a fourth number density, wherein the third coupling elements are respectively electrically conductingly connected to the fourth coupling elements,

- in which the first signal interface is provided along an edge of the first chip and the second signal interface is provided along an edge of the second chip,

- in which the first, second, third and fourth coupling elements are adapted to permit contactless signal transmission between the first and second signal interfaces,

- in which the first and second chips and the coupling component are so arranged relative to each other that third coupling elements of the coupling unit and first coupling elements of the first signal interface and fourth coupling elements of the coupling unit and second coupling elements of the second signal interface can respectively contactlessly transmit signals with each other, wherein said edges of the first and second chips are arranged in mutually facing relationship,

- in which in respect of the longitudinal extents of the first and third coupling elements respectively in the spacing direction of the coupling elements along the line associated therewith, at least one of the longitudinal extents is greater than the length of the overlap of both longitudinal extents,

- in which in respect of the longitudinal extents of the second and fourth coupling elements respectively in the spacing direction of the coupling elements along the line associated therewith, at least one of the longitudinal extents is greater than the length of the overlap of both longitudinal extents,

- and in which the coupling component has a greater number density of coupling elements than the first or the second signal interface or the first and the second signal interfaces.

3. A chip arrangement as set forth in claim 1 or claim 2 in which the first, second and optionally third and fourth coupling elements are adapted to permit contactless signal transmission by means of electromagnetic,

alternatively capacitive, alternatively inductive, alternatively inductive and capacitive coupling between a first and one or more second coupling elements respectively.

4. A chip arrangement as set forth in claim 1 in which the longitudinal extent of that signal interface which has the greater number density is greater.

5. A chip arrangement as set forth in claim 1 in which the second chip at least partially rests on the first chip.

6. A chip arrangement as set forth in claim 2 in which the first and second chips are arranged in mutually juxtaposed relationship on a carrier surface.

7. A chip arrangement as set forth in claim 5 or claim 6 in which a filler with a high dielectric constant is disposed between the first and the second signal interface or optionally between the first signal interface and the coupling unit and between the second signal interface and the coupling unit.

8. A chip arrangement as set forth in one of the preceding claims in which the number N2 of the coupling elements of the signal interface with the greater number density is in the ratio N2=g*N1+X to the number N1 of the coupling elements of the signal interface with the lesser number density, wherein g is a number greater than 1 and X is the number of the coupling elements which are in the overshoot longitudinal portions of the signal interface or optionally the coupling unit.

9. A chip arrangement as set forth in one of the preceding claims in which the signal interface of that chip which in the signal flow between the first and the second chips forms a receiver and is referred to subsequently as the receiver chip has coupling elements with a greater number density.

10. A chip arrangement as set forth in claim 9 comprising a filter circuit on the receiver chip, which is connected downstream of the signal interface and is adapted to reconstruct signals sent from coupling elements at the transmitter end on the basis of the signals received by the coupling elements at the receiver end.

11. A chip arrangement as set forth in claim 10 in which the filter circuit has a number of weighting elements which are respectively adapted to multiply signals received by a plurality of coupling elements at the receiver end by variable weighting factors and to add the signals weighted in that way.

12. A chip arrangement as set forth in claim 11 in which coupling elements at the receiver end are connected to a plurality of weighting elements.

13. A chip arrangement as set forth in claim 11 in which the number of the weighting elements is equal to the number of the coupling elements provided at the transmitter end.

14. A chip arrangement as set forth in claim 11, claim 12 or claim 13 comprising a control unit which is connected to the coupling elements and the filter circuit and is adapted to determine the weighting factors.

15. A chip arrangement as set forth in claim 14 in which the control unit is adapted, for each weighting element, to compare the signals received at the coupling elements at the receiver end which are connected to the filter to a respective predefined signal pattern and to associate a weighting factor dependent on the comparison result with the respective coupling elements.

16. A chip arrangement as set forth in claim 15 in which the control unit is adapted per weighting element to associate a weighting factor which is different from zero at a maximum with one through three coupling elements in such a way that the total of all weighting factors is 1.

17. A chip arrangement as set forth in one of the preceding claims in which the filter circuit additionally or alternatively has a number of filter banks, wherein each filter bank is connected at the input side to a number of coupling elements.

18. A chip arrangement as set forth in claim 17 in which each filter bank has a number of filters and each filter is connected on the input side to a coupling element.

19. A chip arrangement as set forth in claim 18 in which each filter is adapted to deliver an output signal which depends on a weighted sum of the current signal and a number of signals which preceded it in respect of time at its input.

20. A chip arrangement as set forth in claim 17 in which each filter is adapted to determine its output signal A in accordance with the following formula:

$$A(z) = \sum_{j=1}^{r} S(j) \cdot w(j,z)$$

wherein S(j) is a signal at a filter input in a time step j, r is the total number of the time steps considered, w is a weighting factor depending on the respective time step j and z is an index identifying the filter.

21. A chip arrangement as set forth in claim 20 in which the filter has a signal delay line with r delay elements, r multipliers and an adder, wherein a multiplier and a delay element are connected in parallel relationship downstream of each except the last delay element, solely a multiplier is connected downstream of the last delay element, and the

outputs of the multipliers are connected to parallel inputs of the summing member.

22. A chip arrangement as set forth in claims 18 through 21 in which each filter bank has a weighting unit which is adapted to multiply signals received by the filters of the respective filter bank by variable weighting factors and to add the signals weighted in that way.

23. A chip arrangement as set forth in one of claims 17 through 22 comprising a control unit which is connected to the filter banks and which is adapted in a training phase to subject the signals applied to the coupling elements at the receiver end to correlation with one or more known signal patterns and on the basis of the correlation result to determine the weighting factors of the filters and the weighting circuit.

24. A chip arrangement as set forth in one of the preceding claims in which the chip without an increased number of first coupling elements has a respective edge coupling element at the ends of its signal interface and is adapted to apply a predefined edge signal to the edge coupling elements.

25. A chip arrangement as set forth in claim 1 or claim 2 in which that chip which forms a transmitter in the signal flow between the first and the second chips has a transmitting circuit which has complementary CMOS transistors.

26. A chip arrangement as set forth in claim 1 or claim 2 in which a chip is a microprocessor and the other chip is a memory chip.

27. A chip arrangement as set forth in claim 1 comprising a third chip which is coupled to the first chip or the second chip corresponding to the manner recited in claim 1 or claim 2 for signal transmission in such a way that the first or the second chip respectively is adapted for coupling to the third chip like the first chip of claim 1 or claim 2 and the third chip is

adapted for coupling to the first chip like the second chip of claim 1 or claim 2, or vice-versa, wherein the first or the second chip has a further signal interface having the features of the first signal interface or the second signal interface.

28. A chip arrangement as set forth in claim 2 comprising a third chip which with the first or the second chip corresponding to the manner recited in claim 1 or claim 2 is adapted and arranged for signal transmission, wherein the first or the second chip has a further signal interface having the features of the first signal interface or the second signal interface.

29. A coupling component for contactless signal transmission between a first and a second chip in an arrangement as set forth in claim 2, which on a substrate has a coupling unit which has third coupling elements arranged along a third line in a third number density and fourth coupling elements arranged along a fourth line in a fourth number density, wherein the third coupling elements are respectively electrically conductingly connected to the fourth coupling elements.

30. A coupling component as set forth in claim 29 in which the spacing of the third or fourth coupling elements and their widthwise extent are so selected that a third coupling element or a fourth coupling element and the spacing relative to an adjacent third or fourth coupling element respectively assume overall a maximum of 10 micrometers.

31. A chip for use in an arrangement as set forth in claim 1 or claim 2 which has at least one first signal interface with first coupling elements arranged along a first line in a first number density or at least one second signal interface with second coupling elements arranged along a second line in a second number density or which has at least one first and at least one second signal interface, and in which the first and optionally the second signal interface is arranged along an edge of the chip.

32. A chip as set forth in claim 31 in which the first or the second coupling elements are metallic electrically conductive strips arranged in mutually parallel relationship.

33. A chip as set forth in claim 32 in which the sum of the spacing and the strip width is between 1 and 25 micrometers.

34. A chip as set forth in claim 31 in which the coupling elements are coils whose magnetic longitudinal axes are arranged in a horizontal plane in parallel relationship with the surface of the chip.

35. A chip as set forth in claim 31 in which the first coupling elements, alternatively the second coupling elements, alternatively the first and second coupling elements, are covered by an insulating layer.

36. A chip as set forth in claim 31 having a reference edge for positioning in a chip arrangement.

37. A chip as set forth in one of claims 31 through 36 having the additional features of one of claims 10 through 29.

38. A chip as set forth in claim 31 in which a respective metal element which is connected to ground is provided between the first coupling elements.

39. A chip as set forth in claim 38 in which the metal element surrounds the coupling element laterally and at the substrate side, in particular in a U-shape.

40. A chip as set forth in claim 31 comprising a transmitter control which is adapted to output signals on adjacent first or second coupling elements with a predetermined phase shift relative to each other.

41. A wafer for the production of a chip as set forth in claim 31 comprising a plurality of chip portions, wherein at least one chip portion has the features of a chip as set forth in claim 31.

42. A process for the production of a chip arrangement as set forth in claim 2 comprising the steps:

a) positioning the first chip on a carrier,

b) positioning the second chip relative to the first chip on the carrier,

c) positioning a coupling component to produce a contactless coupling for signal transmission between the first and second chips.

43. A process as set forth in claim 42 comprising an additional step of ascertaining active coupling elements.